

MECHANICAL COOLING FIN FOR INTERCONNECTS

FIELD OF INVENTION

[0001] This invention relates to integrated circuits and more particularly to an integrated circuit providing thermally conductive electrically inactive extensions to active interconnect lines to reduce localized Joule heating in interconnect lines.

BACKGROUND OF INVENTION

[0002] Typical semiconductor devices comprise multiple circuits formed within a dielectric region comprised of one or more dielectric layers on top of a silicon substrate or wafer. On top of the substrate are layers of dielectric and layers of metal and layers of metal embedded in dielectric. When the metal interconnect leads of the circuits are on different layers, conductive vias extend through the dielectric layers to make connections between the wiring leads on different interconnect levels. Sometimes, based on the circuit design, a significantly large amount of current may flow through the metal interconnect lead, causing Joule heating to increase the temperature of the metal lead. The current flowing through these leads may cause sufficient Joule heating to increase the temperature of the lead. Such temperature increases may accelerate reliability wearout mechanisms such as electromigration and stress migration that might possibly lead to failure of the integrated circuit. It is common practice to widen leads that have current densities in excess of those required for reliable operation. However, widening leads may have a deleterious impact on the area of the integrated circuit.

[0003] Current trends in integrated circuit design include using dielectric materials of increasingly low thermal conductivity, exacerbating the deleterious effects of Joule heating within the integrated circuit. In addition, as integrated circuit technologies are scaled, the number of layers of metal interconnect is increasing, making it increasingly difficult to dissipate heat from metal leads. Furthermore, integrated circuits that draw relatively large amounts of power may intensify the increases in temperature in the integrated circuit due to Joule heating effects.

[0004] During fabrication of integrated circuits, dummy metal structures may be inserted in the integrated circuit to increase the density of metal structures on the top surface of the integrated circuit. For example, insertion of dummy metal structures may lead to improved pattern consistency of metal leads and to reduced "dishing" during chemical mechanical polishing (CMP) of the integrated circuit. It is common practice to use dummy metal structures during the fabrication of integrated circuits. Because metals are much better thermal conductors than are dielectrics, the presence of dummy metal structures surrounding regions where the temperatures of metal leads may become excessive can contribute to heat flow away from such interconnect region toward heat sinking regions, thereby resulting in lower temperatures of the metal leads. Vertical vias may be formed within the dielectric layer between dummy metal structures and filled with a thermally conductive material to provide direct thermal connections between dummy metal structures. Although this may help dissipate heat from metal leads or other heat generating structures, such techniques may still be inadequate for integrated circuit applications. An integrated circuit with such heat conductive structures is described in co-pending patent application of Hunter et al. entitled "Integrated Circuit Providing

Thermally Conductive Structures Substantially Horizontally Coupled To One Another Within One or More Heat Dissipation Layers To Dissipate Heat From A Heat Generating Structure”, serial no. (TI-33209) filed December 20, 2002. This application is incorporated herein by reference.

SUMMARY OF INVENTION

[0005] According to an embodiment of the present invention, electrically inactive extensions of electrically active interconnect leads are fabricated. The term electrically inactive as used herein means that they are not connected to anything else, and therefore do not conduct any nominal current. The purpose of these electrically inactive extensions are to more efficiently conduct heat to regions of the integrated circuit design where heat can flow to heat sinking regions of the integrated circuit, such as the substrate upon which the integrated circuit is fabricated. Each extension can be thought of as a micro-miniature thermal cooling fin. The position of each thermal cooling fin can be optimized with respect to its size and nearness to the substrate and to other dummy metal structures.

DESCRIPTION OF DRAWINGS

[0006] Figure 1 illustrates a top plan view of embodiments described in connection with Figs. 2-7 of the present invention of an electrically active line and an electrically inactive cooling fin.

[0007] Figure 2 illustrates a cross section of Figure 1 taken through A-A for one embodiment of the present invention.

[0008] Figure 3 illustrates a cross section of Figure 1 taken through B-B for the embodiment of Fig. 2.

[0009] Figure 4 illustrates a cross section taken through A-A of Figure 1 wherein the electrically inactive cooling fin is positioned multiple layers below the electrically active line.

[0010] Figure 5 illustrates a cross section taken through B-B of Figure 1 wherein the electrically inactive cooling fin is positioned multiple layers below the electrically active line.

[0011] Figure 6 illustrates a cross section view of Fig. 1 taken through A-A wherein the cooling fin is on the on the same surface as the via in Figs. 2 and 3.

[0012] Figure 7 illustrates a perspective view of the case where the mechanical cooling fin is in the shape of an “H” and is in the same heat dissipating layer as the via In Fig. 2 and 3 for a single damascene process.

[0013] Figure 8 illustrates a top plan view of an embodiment described in connection with Figs. 9-10 of the present invention of an electrically active line and an electrically inactive cooling fin with dummy metal structures.

[0014] Figure 9 illustrates a cross section taken through A-A of Figure 8 wherein the dielectric region contains layers of dummy metal and the electrically inactive cooling fin is aligned to overlay on top of underlying dummy metal in accordance with another embodiment of the present invention.

[0015] Figure 10 illustrates a cross section taken through B-B of Figure 8 wherein the dielectric region contains layers of dummy metal and the electrically inactive cooling fin

is aligned to overlay on top of underlying dummy metal in accordance with the same embodiment of the present invention as Fig. 9.

DESCRIPTION OF PREFERRED EMBODIMENT

[0016] Figures 1-3 shows one embodiment of the present invention for reducing the temperature rise due to Joule heating. Figure 1 is a top plan view of the integrated circuit 10 according to embodiments of the present invention described in connection with Figs. 2-7. Figure 2 is a cross section taken through A-A in Figure 1 and Figure 3 is an orthogonal cross section taken through B-B in Figure 1. The integrated circuit 10 includes a substrate 24 of silicon, for example, having a top surface 26 and bottom surface 28 and dielectric region or layer 18 above the substrate 24 with a bottom surface 22 adjacent with the top surface 26 of the substrate 24. The dielectric region or layer 18 may include silicon dioxide, silicon nitride, or other suitable dielectric material. The dielectric region or layer 18 comprises multiple layers of heat generating leads or other structures embedded within the dielectric region 18, such as an electrically active current carrying metal lead 13 in layer 18a. The metal lead 13 is represented by dashed lines in Figure 1 since the lead 13 is in a layer 18a below the top surface of the dielectric. The heat generating electrically active current carry metal lead may include copper, aluminum tungsten, or other suitable metal or metal alloy. The dielectric region 18 has at least one of its two surfaces - top and bottom - thermally coupled to an external heat sink by virtue of its packaging details. For simplicity, we will refer to the case where heat flow is through the bottom surface 22 connection to the integrated circuit substrate 24 at the top surface 26, although it is understood that the invention applies to the case where the other or both surfaces are thermally coupled to heat sinks. There should be external heart sinks, as part of the details of integrated circuit packaging and the mounting of packages in the systems.

[0017] In accordance with one embodiment of the present invention thermal cooling conductor or fin 14 is located in a substantially horizontal region 17a in the dielectric region 18 below an interconnect connector 13 layer 18a. This cooling fin is represented by dashed lines in Figure 1 since this is also below the top surface. The cooling fin 14 is physically connected to the electrically active interconnect conductor 13 to help dissipate the heat generated in the electrically active interconnect conductor 13. The thermal cooling conductor or fin 14 includes electrically inactive metal conductor such as a straight heat conductive line 14 physically connected by a connecting conductor via 15 extending in layer 18b between layers 18a and 17a to the electrically active interconnect lead 13 in which Joule heat is being generated. Only a portion of the electrically active interconnect lead 13 is shown in the Figures 1-3.

[0018] The electrical inactivity of cooling fin 14 means that it is not connected to any other portion of electrically active interconnect, and therefore does not carry any intentional current. It is also to be understood that the shape of the cooling fin 14 does not have to be a straight line. It is also to be understood that the cooling fin 14 does not have to be constrained to a specific size. It can be any shape and size that is convenient while considering the tradeoffs between impact on circuit layout, circuit performance, and thermal management.

[0019] This above described arrangement is a preferred embodiment because it places the cooling fin 14 as close as possible to the heat sinking substrate 24, thereby optimizing heat loss from the active metal. Alignment with other electrically inactive metal structures, such as dummy metal, may also optimize heat loss and consequent temperature reduction.

[0020] In the case where the dominant heat sink direction is above the dielectric region 18 or for other reasons, the electrically inactive cooling fin 14 would be in a layer above the electrically active interconnect 13 and the placement of the elements in Figs. 1-3 would be reversed with fin 14 closer to the top of the dielectric region 18 where the top heat sink is located in place of active interconnect 13 and the location of the interconnect line 13 would be below the and in place of fin 14 in Figs. 2 and 3.

[0021] In general, the electrically active interconnect lead can be connected to a cooling fin which is on ant level above or below. Whether it is above or below depends on whether the dominant heat sinking direction is above or below the dielectric region 18, respectively. As an example, in the case where the dominant heat sinking direction is through the substrate 24, there may be multiple vias 15 between the electrically active interconnect lead 13 and the inactive cooling fin 14 as illustrated in Figures 4 and 5. Figures 4 and 5 are cross sections of Figure 1 taken at planes A-A for Figure 4 and plane B-B for Figure 5. The connection between the two vias 15 may include a conductive pad or block 17 at layer 18a. The closer the cooling fin 14 can be placed to the heat sinking substrate 24 for example the more optimal will be the temperature reduction of the electrically active lead. If on the other hand the heat sinking surface is at the top, the closer to the top the better.

[0022] In accordance with another embodiment of the present invention, the electrically inactive heat dissipating cooling fin 14 is built in the same layer 18b as was the via 15 in Fig. 1-3, by extending the normal via pattern to have an extended via shape. This is illustrated in Figure 6 for the case where the electrically inactive cooling fin 14 is below the electrically active interconnect lead 13 in the same plane as the via 15 in Figs.

1-3. Figure 6 illustrates the A-A cross section of Figure 1. The thermal cooling fin 14 may be formed in the surrounding dielectric layer 18b during the same single damasene process as is the via 15 in Figs. 1-3, wherein holes are formed in the surrounding dielectric layer 18b and filled with copper and then polished off to the surface of the dielectric layer. It is to be understood that the cooling fin 14 could also have been fabricated above the electrically active interconnect lead 13.

[0023] The shape of the cooling fin 14 may be other than a straight line and as shown by the perspective view in Figure 7 to provide the cooling surface. Any shape consistent with via design rule constraints could be patterned. In Figure 7 the electrically inactive cooling fin 14 extends out in the shape of an “H” with two conductors 14a and 14b parallel to the interconnect line 13 and a cross connective and conductive bar 14c orthogonal and connected to conductors 14a and 14b, with the cross bar 14c across the interconnect lead 13 and connected thereto. Heat flow from the line 13 to the fin occurs in the overlap region between the line 13 and the crossbar 14c, where the two layers are in contact. The extension of the interconnect line 13 in Figure 7 is not solid so as to illustrate the fin 14.

[0024] In accordance with another embodiment of the present invention, the electrically inactive heat dissipating cooling fin 14 is built in the same layer as the electrically active interconnect line 13 and is in fact a heat dissipating stub connection off the active line. The shape can be other than a straight line. extending and fabricated when the interconnect line is formed. The fins have to be designed so as not to interfere with the other electrical lines, and in a manner that has acceptable parasitic capacitance.

[0025] The presence of dummy metal structures increases the conductivity of heat to the substrate 11 and a heat sink. The electrically inactive cooling fin may be lined up with dummy metal structures 33 as illustrated in Figures 8,9 and 10. In Figure 8 and 9 the electrically inactive cooling fin 14 extends along several dummy metal structures 33 below the cooling fin that aid in the conduction of the heat to the substrate 11. In Figure 8 these dummy metal structures 33 are represented by dashed lines because they are below and aligned with the upper dummy metal structures 30 and the cooling fin 14. In Figure 10 the electrically inactive cooling fin 14 is lined up with a dummy metal structure 33 that is located between the cooling fin 14 and the substrate 11.

[0026] Although the system and method of the present invention has been described in connection with the preferred embodiment, it is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention as defined by the appended claims.